# CEP703AL/CEB703AL
# CEP703ALZ/CEB703ALZ
# CEP703ALG/CEB703ALG

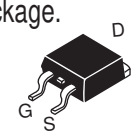
4

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

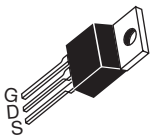
March 1998

## FEATURES

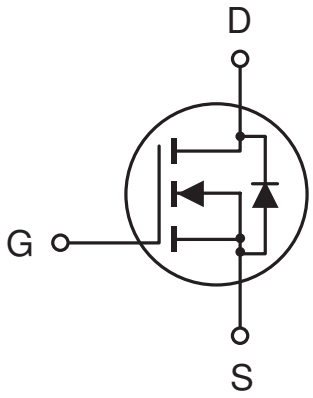
- 30V , 40A , $R_{DS(ON)}$=17mΩ @$V_{GS}$=10V.
  $R_{DS(ON)}$=30mΩ @$V_{GS}$=4.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- The character "Z" represents the "Lead free".
- The character "G" represents the "Green package".
- TO-220 & TO-263 package.




CEB SERIES
TO-263(DD-PAK)




CEP SERIES
TO-220




## ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 30 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current-Continuous[a] @$T_J$=125°C | $I_D$ | 40 | A |
| -Pulsed | $I_{DM}$ | 120 | A |
| Drain-Source Diode Forward Current[a] | $I_S$ | 40 | A |
| Maximum Power Dissipation[a] @Tc=25°C | $P_D$ | 50 | W |
| Derate above 25°C | | 0.4 | W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{STG}$ | -65 to 175 | °C |

## THERMAL CHARACTERISTICS

| | | | |
|---|---|---|---|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 3 | °C/W |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 62.5 | °C/W |

## ELECTRICAL CHARACTERISTICS (Tc 25°C unless otherwise noted)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250μA | 30 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 24V, $V_{GS}$ = 0V | | | 1 | μA |
| Gate-Body Leakage | $I_{GSS}$ | $V_{GS}$ = ±20V, $V_{DS}$ = 0V | | | ±100 | nA |
| **ON CHARACTERISTICS**[a] | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 1 | 1.7 | 3 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$ = 10V, $I_D$ = 25A | | 14 | 17 | mΩ |
| | | $V_{GS}$ = 4.5V, $I_D$ = 10A | | 22 | 30 | mΩ |
| On-State Drain Current | $I_{D(ON)}$ | $V_{GS}$ = 10V, $V_{DS}$ = 10V | 60 | | | A |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 10V, $I_D$ = 25A | | 30 | | S |
| **DYNAMIC CHARACTERISTICS**[b] | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ =15V, $V_{GS}$ = 0V<br>f =1.0MHz | | 1005 | | pF |
| Output Capacitance | $C_{OSS}$ | | | 420 | | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | 100 | | pF |
| **SWITCHING CHARACTERISTICS**[b] | | | | | | |
| Turn-On Delay Time | $t_{D(ON)}$ | $V_{DD}$ = 15V,<br>$I_D$ =25A,<br>$V_{GS}$ = 10V,<br>$R_{GEN}$ =24Ω | | 18 | 23 | ns |
| Rise Time | $t_r$ | | | 120 | 180 | ns |
| Turn-Off Delay Time | $t_{D(OFF)}$ | | | 80 | 120 | ns |
| Fall Time | $t_f$ | | | 60 | 165 | ns |
| Total Gate Charge | $Q_g$ | $V_{DS}$ =10V, $I_D$ = 25A,<br>$V_{GS}$ =5V | | 15 | 20 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | 3 | | nC |
| Gate-Drain Charge | $Q_{gd}$ | | | 7 | | nC |

# CEP703AL/CEB703AL
# CEP703ALZ/CEB703ALZ
# CEP703ALG/CEB703ALG

## ELECTRICAL CHARACTERISTICS ($T_C$=25°C unless otherwise noted)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DRAIN-SOURCE DIODE CHARACTERISTICS** [b] | | | | | | |
| Diode Forward Voltage | $V_{SD}$ | $V_{GS}$ = 0V, Is =25A | | 0.93 | 1.3 | V |

Notes

a.Pulse Test:Pulse Width ≤300 μs, Duty Cycle ≤ 2%.
b.Guaranteed by design, not subject to production testing.

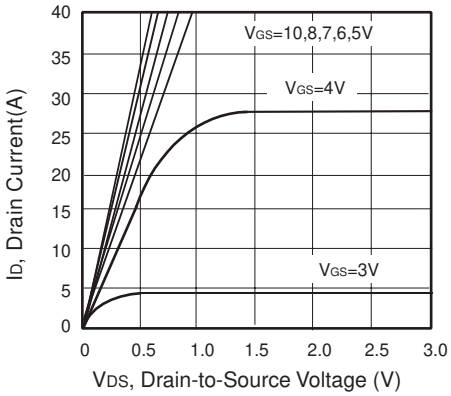



**Figure 1. Output Characteristics**

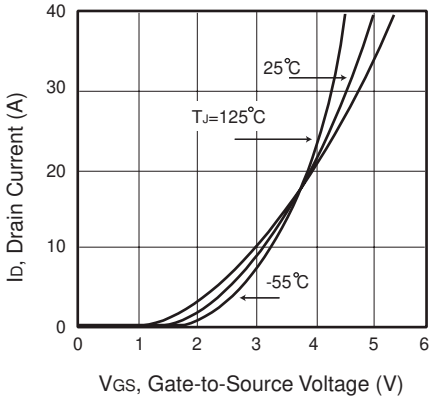



**Figure 2. Transfer Characteristics**

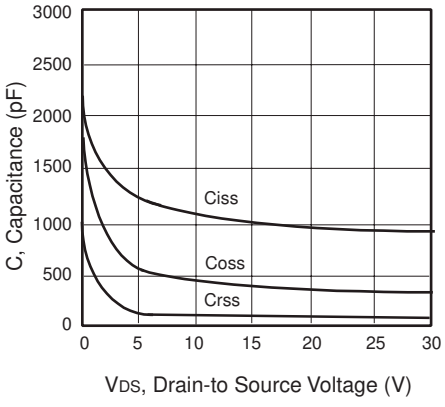



**Figure 3. Capacitance**

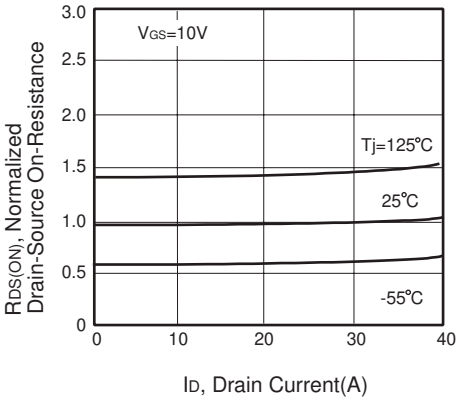



**Figure 4. On-Resistance Variation with Drain Current and Temperature**

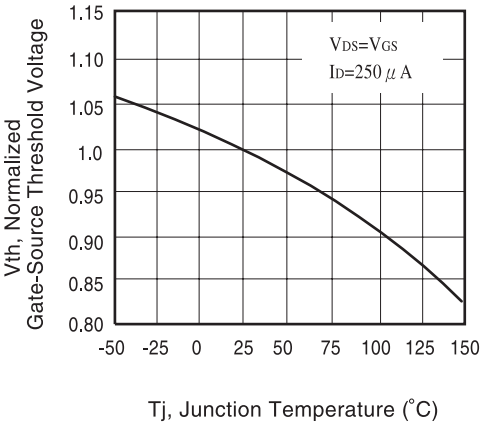



**Figure 5. Gate Threshold Variation with Temperature**

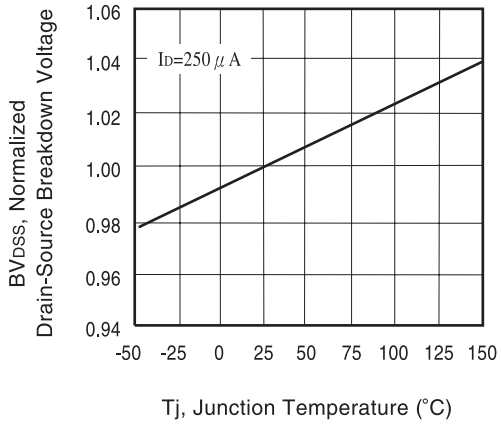



**Figure 6. Breakdown Voltage Variation with Temperature**

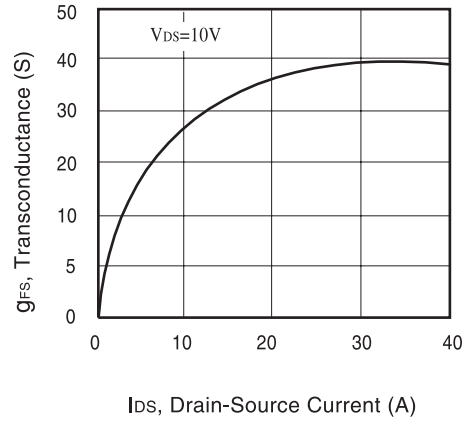



**Figure 7. Transconductance Variation with Drain Current**

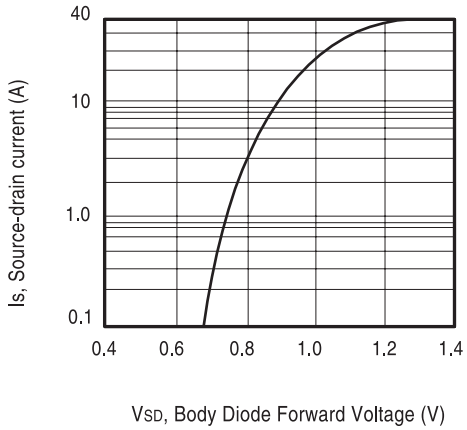



**Figure 8. Body Diode Forward Voltage Variation with Source Current**

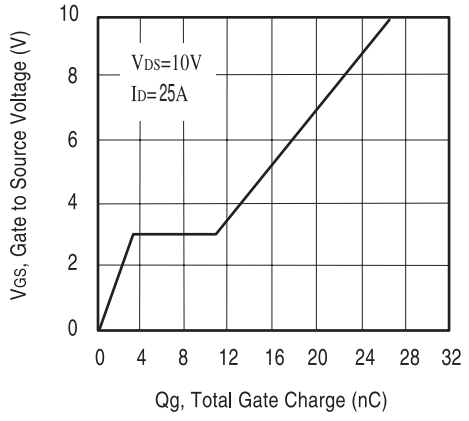



**Figure 9. Gate Charge**

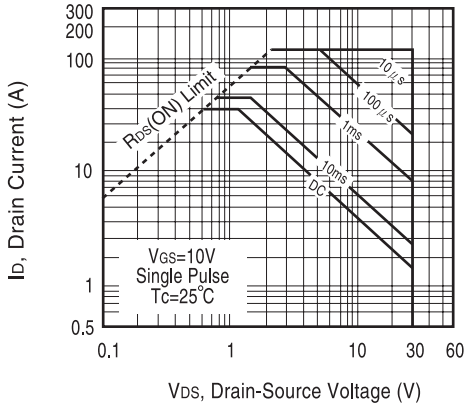



**Figure 10. Maximum Safe Operating Area**

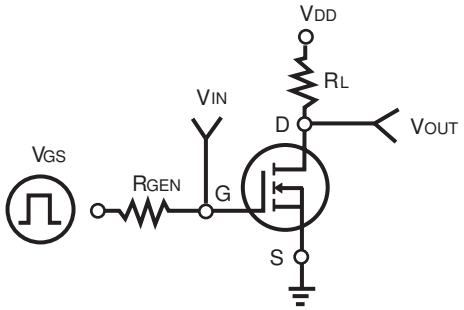



**Figure 11. Switching Test Circuit**

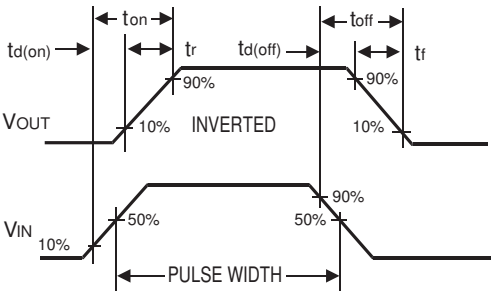



**Figure 12. Switching Waveforms**

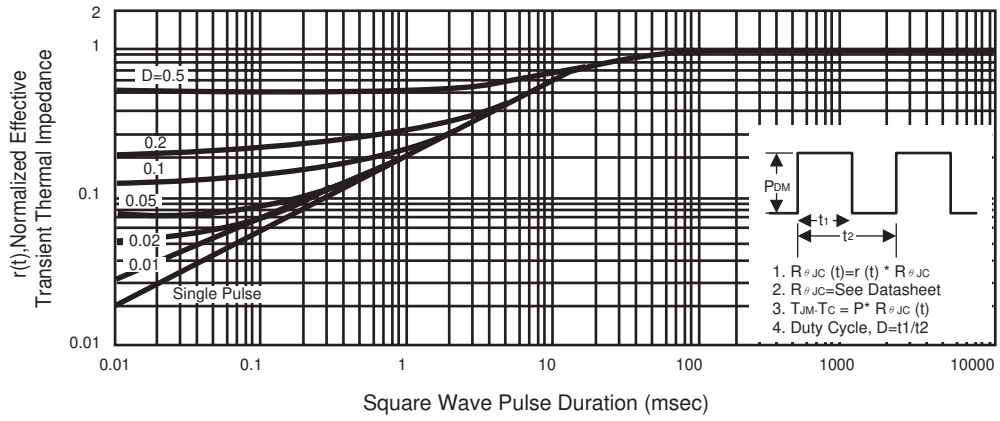



**Figure 13. Normalized Thermal Transient Impedance Curve**